

IN THE CLAIMS

Please amend claims 1, 13-14, 16, 22, 25, 27-29, 31-32, 34, 36-41, and 43-52 as follows below.

Please cancel claims 2-3, 17, 19, 21, 26, 35, 42, and 58-72 without prejudice.

Please add new claims 73-80 as follow below.

This listing of claims will replace all prior versions, and listings, of claims in the application:

MARKED UP VERSION OF CLAIMS

1           1. (Currently Amended) A method of processing for a  
2 semiconductor device, the method comprising:  
3           providing a wafer including a substrate;  
4           forming a plurality of sidewalls around a plurality of  
5 cylindrical pedestals above a surface of the substrate;  
6           removing the plurality of cylindrical pedestals; and  
7           vertically etching horizontal surfaces of a first  
8 material located around the plurality of sidewalls, wherein  
9 the plurality of sidewalls provide an etch stop and protect  
10 the first material under the plurality of sidewalls from  
11 being etched during the vertical etching of the first  
12 material.

1           2. (Cancelled)

1           3. (Cancelled)

1           4. (Original) The method of claim 1, further comprising:

2 removing the plurality of sidewalls.

1 5. (Original) The method of claim 1, further comprising:  
2 diffusing a dopant into the first material located  
3 around the plurality of sidewalls.

1 6. (Original) The method of claim 1, further comprising:  
2 diffusing a dopant into a second material around the  
3 plurality of sidewalls.

1 7. (Original) The method of claim 1, further comprising:  
2 diffusing a dopant into the first material and a  
3 second material around the plurality of sidewalls.

1 8. (Original) The method of claim 1, further comprising:  
2 diffusing a dopant into the first material or a second  
3 material around the plurality of sidewalls.

1 9. (Original) The method of claim 8, wherein,  
2 the plurality of sidewalls provide an etch stop and a  
3 diffusion barrier.

1 10. (Original) The method of claim 9, wherein,  
2 the plurality of sidewalls protect the first material  
3 under the plurality of sidewalls from receiving a dopant  
4 during the diffusing of the dopant into the first material  
5 or the second material.

1 11. (Original) The method of claim 9, wherein,

2           the plurality of sidewalls protect the second material  
3           under the plurality of sidewalls from receiving a dopant  
4           during the diffusing of the dopant into the first material  
5           and the second material.

1           12. (Original) The method of claim 9, wherein,  
2           the plurality of sidewalls protect the first material  
3           and the second material under the plurality of sidewalls  
4           from receiving a dopant during the diffusing of the dopant  
5           into the first material or the second material.

1           13. (Withdrawn-Currently Amended) A method of processing  
2           for a semiconductor device, the method comprising:  
3           providing a wafer including a substrate;  
4           forming a plurality of sidewalls around a plurality of  
5           cylindrical pedestals above a surface of the substrate;  
6           removing the plurality of cylindrical pedestals;  
7           vertically etching horizontal surfaces of a first  
8           material located around the plurality of sidewalls, wherein  
9           the plurality of sidewalls provide an etch stop and protect  
10           the first material under the plurality of sidewalls from  
11           being etched during the vertical etching of the first  
12           material; and  
13           diffusing a dopant into the [[a]] first material  
14           located around the plurality of sidewalls.

1           14. (Withdrawn-Currently Amended) The method of claim 13,  
2           wherein,  
3           the plurality of sidewalls further provide a diffusion  
4           barrier.

1        15. (Withdrawn) The method of claim 14, wherein,  
2            the plurality of sidewalls protect the first material  
3        under the plurality of sidewalls from receiving a dopant  
4        during the diffusing of the dopant into the first material.

1        16. (Withdrawn-Currently Amended) The method of claim 13,  
2 further comprising:  
3            removing at least one of the plurality of sidewalls.

1        17. (Withdrawn-Cancelled)

1        18. (Withdrawn) The method of claim 13, further comprising:  
2            vertically etching horizontal surfaces of a second  
3        material located around the plurality of sidewalls.

1        19. (Withdrawn-Cancelled)

1        20. (Withdrawn) The method of claim 13, further comprising:  
2            vertically etching horizontal surfaces of the  
3        substrate located around the plurality of sidewalls.

1        21. (Withdrawn-Cancelled)

1        22. (Withdrawn-Currently Amended) The method of claim  
2 [[21]] 18, wherein,  
3            the plurality of sidewalls further provide a diffusion  
4        barrier ~~and an etch stop~~.

1        23. (Withdrawn) The method of claim 22, wherein,  
2            the plurality of sidewalls protect the first material  
3        under the plurality of sidewalls from being etched during  
4        the etching of the first material.

1        24. (Withdrawn) The method of claim 22, wherein,  
2            the plurality of sidewalls protect the second material  
3        under the plurality of sidewalls from being etched during  
4        the etching of the second material.

1        25. (Withdrawn-Currently Amended) The method of claim  
2        [[22]] 18, wherein,  
3            the plurality of sidewalls protect the first material  
4        and the second material under the plurality of sidewalls  
5        from being etched during the vertical etching of the first  
6        material and the second material.

1        26. (Withdrawn-Cancelled)

1        27. (Withdrawn-Currently Amended) A method of processing  
2        for a semiconductor device, the method comprising:  
3            providing a wafer including a substrate of the  
4        semiconductor device;  
5            forming a plurality of sidewalls around a plurality of  
6        cylindrical pedestals above a surface of the substrate;  
7            removing the plurality of cylindrical pedestals;  
8            vertically etching horizontal surfaces of a first  
9        material located around the plurality of sidewalls, wherein  
10        the plurality of sidewalls provide an etch stop and protect

11        the first material under the plurality of sidewalls from  
12        being etched during the vertical etching of the first  
13        material; and  
14        diffusing a dopant around the plurality of sidewalls.

1        28. (Withdrawn-Currently Amended) The method of claim 27,  
2        wherein,  
3                the plurality of sidewalls are formed by  
4                forming [[a]] the plurality of cylindrical pedestals  
5                above [[a]] the surface of the substrate,  
6                depositing a sidewall material layer over the  
7                cylindrical pedestals and the substrate,  
8                vertically etching the horizontal surfaces of the  
9                sidewall material,  
10               and  
11               the plurality of cylindrical pedestals are removed by  
12        etching away the plurality of cylindrical pedestals.

1        29. (Withdrawn-Currently Amended) The method of claim 27,  
2        wherein,  
3                the vertical etching of horizontal surfaces of the  
4                first material located around the plurality of sidewalls is  
5                performed using a substantially anisotropic etchant.

1        30. (Withdrawn) The method of claim 27, wherein,  
2                the plurality of sidewalls provide an etch stop and a  
3                diffusion barrier.

1        31. (Withdrawn-Currently Amended) The method of claim 30,  
2        wherein,

3           the plurality of sidewalls protect the first material  
4           under the plurality of sidewalls from being etched during  
5           the etching of the first material around the plurality of  
6           sidewalls and the plurality of sidewalls protect the first  
7           material under the plurality of sidewalls from receiving  
8           the dopant during the diffusing of the dopant around the  
9           plurality of sidewalls.

1           32. (Withdrawn-Currently Amended) A method of processing  
2           for a semiconductor device, the method comprising:

3           providing a wafer including a substrate of the  
4           semiconductor device, the semiconductor device being a  
5           transistor or a diode;

6           forming a plurality of sidewalls around a plurality of  
7           cylindrical pedestals above a surface of the substrate;

8           removing the plurality of cylindrical pedestals;

9           vertically etching horizontal surfaces of a first  
10          material located around the plurality of sidewalls, wherein  
11          the plurality of sidewalls provide an etch stop and protect  
12          the first material under the plurality of sidewalls from  
13          being etched during the vertical etching of the first  
14          material; and

15          diffusing a dopant around the plurality of sidewalls.

1           33. (Withdrawn) The method of claim 32, wherein,  
2           the plurality of sidewalls provide a diffusion  
3           barrier.

1           34. (Withdrawn-Currently Amended) The method of claim 32,  
2           wherein,

3           the plurality of sidewalls are formed by  
4           forming [[a]] the plurality of cylindrical pedestals  
5       above [[a]] the surface of the substrate,  
6           depositing a sidewall material layer over the  
7       cylindrical pedestals and the substrate,  
8           vertically etching the horizontal surfaces of the  
9       sidewall material,  
10          and  
11          the plurality of cylindrical pedestals are removed by  
12       etching away the plurality of cylindrical pedestals.

1       35. (Withdrawn-Cancelled)

1       36. (Withdrawn-Currently Amended) The method of claim  
2       [[35]] 32, wherein,  
3           the plurality of sidewalls provide an etch stop and a  
4       diffusion barrier.

1       37. (Withdrawn-Currently Amended) The method of claim  
2       [[35]] 32, wherein,  
3           the vertical etching of horizontal surfaces of the  
4       first material located around the plurality of sidewalls is  
5       performed using a substantially anisotropic etchant.

1       38. (Withdrawn-Currently Amended) The method of claim 36,  
2       wherein,  
3           the plurality of sidewalls protect the first material  
4       under the plurality of sidewalls from being etched during  
5       the vertical etching of horizontal surfaces of the first  
6       material around the plurality of sidewalls and the



7 plurality of sidewalls protect the first material under the  
8 plurality of sidewalls from receiving the dopant during the  
9 diffusing of the dopant around the plurality of sidewalls.

1 39. (Withdrawn-Currently Amended) The method of claim 35,  
2 wherein,

3 the first material located around the plurality of  
4 sidewalls which is vertically etched is the substrate.

1 40. (Withdrawn-Currently Amended) The method of claim 35,  
2 wherein,

3 the first material located around the plurality of  
4 sidewalls which is vertically etched is a layer exposed  
5 over a surface of the substrate and protected under the  
6 plurality of sidewalls.

1 41. (Withdrawn-Currently Amended) A method of processing  
2 for a semiconductor device, the method comprising:

3 providing a wafer including a substrate of the  
4 semiconductor device, the semiconductor device being a  
5 transistor or a diode;

6 forming a plurality of sidewalls around a plurality of  
7 cylindrical pedestals above a surface of the substrate;

8 removing the plurality of cylindrical pedestals; and  
9 vertically etching horizontal surfaces of a first

10 material located around the plurality of sidewalls, wherein  
11 the plurality of sidewalls provide an etch stop and protect  
12 the first material under the plurality of sidewalls from  
13 being etched during the vertical etching of the first  
14 material.

1           42. (Withdrawn-Cancelled)

1           43. (Withdrawn-Currently Amended) The method of claim 41,  
2 wherein,

3           the first material located around the plurality of  
4           sidewalls which is horizontally etched is the substrate.

1           44. (Withdrawn-Currently Amended) The method of claim 41,  
2 wherein,

3           the first material located around the plurality of  
4           sidewalls which is horizontally etched is an epitaxial  
5           layer of the substrate.

1           45. (Withdrawn-Currently Amended) The method of claim 41,  
2 wherein,

3           the first material located around the plurality of  
4           sidewalls which is horizontally etched is a layer exposed  
5           over a surface of the substrate and protected under the  
6           plurality of sidewalls.

1           46. (Withdrawn-Currently Amended) The method of claim 41,  
2 wherein,

3           the vertical etching of horizontal surfaces of the  
4           first material located around the plurality of sidewalls is  
5           performed using a substantially anisotropic etchant.

1           47. (Withdrawn-Currently Amended) The method of claim 41,  
2 wherein,

3           the plurality of sidewalls are formed by

4           forming ~~[[a]]~~ the plurality of cylindrical pedestals  
5           above ~~[[a]]~~ the surface of the substrate,  
6           depositing a sidewall material layer over the  
7           cylindrical pedestals and the substrate,  
8           vertically etching the horizontal surfaces of the  
9           sidewall material,  
10          and  
11          the plurality of cylindrical pedestals are removed by  
12          etching away the plurality of cylindrical pedestals.

1           48. (Withdrawn-Currently Amended) The method of claim 41,  
2           further comprising:

3                  implanting ~~diffusing~~ a dopant around the plurality of  
4           sidewalls.

1           49. (Withdrawn-Currently Amended) The method of claim 48,  
2           wherein,

3                  the plurality of sidewalls provide an etch stop and a  
4           ~~diffusion~~ barrier.

1           50. (Withdrawn-Currently Amended) The method of claim 49,  
2           wherein,

3                  the plurality of sidewalls protect the first material  
4           under the plurality of sidewalls from being etched during  
5           the vertical etching of the first material located around  
6           the plurality of sidewalls and the plurality of sidewalls  
7           protect the first material under the plurality of sidewalls  
8           from receiving the dopant during the diffusing of the  
9           dopant around the plurality of sidewalls.

1           51. (Withdrawn-Currently Amended) The method of claim 48,  
2 wherein,  
3           the dopant is ~~diffused~~ implanted into the substrate  
4           around the plurality of sidewalls.

1           52. (Withdrawn-Currently Amended) The method of claim 48,  
2 wherein,  
3           the dopant is ~~diffused~~ implanted into the first  
4           material around the plurality of sidewalls.

1           53-72. (Cancelled)

1           73. (New) The method of claim 6, wherein  
2           the plurality of sidewalls provide an etch stop and a  
3           diffusion barrier.

1           74. (New) The method of claim 73, wherein  
2           the plurality of sidewalls protect the first material  
3           under the plurality of sidewalls from receiving a dopant  
4           during the diffusing of the dopant into the first material  
5           or the second material.

1           75. (New) The method of claim 73, wherein  
2           the plurality of sidewalls protect the second material  
3           under the plurality of sidewalls from receiving a dopant  
4           during the diffusing of the dopant into the first material  
5           and the second material.

1        76. (New) The method of claim 73, wherein,  
2            the plurality of sidewalls protect the first material  
3        and the second material under the plurality of sidewalls  
4        from receiving a dopant during the diffusing of the dopant  
5        into the first material or the second material.

1        77. (New) The method of claim 7, wherein  
2            the plurality of sidewalls provide an etch stop and a  
3        diffusion barrier.

1        78. (New) The method of claim 77, wherein  
2            the plurality of sidewalls protect the first material  
3        under the plurality of sidewalls from receiving a dopant  
4        during the diffusing of the dopant into the first material  
5        or the second material.

1        79. (New) The method of claim 77, wherein  
2            the plurality of sidewalls protect the second material  
3        under the plurality of sidewalls from receiving a dopant  
4        during the diffusing of the dopant into the first material  
5        and the second material.

1        80. (New) The method of claim 77, wherein,  
2            the plurality of sidewalls protect the first material  
3        and the second material under the plurality of sidewalls  
4        from receiving a dopant during the diffusing of the dopant  
5        into the first material or the second material.